This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): A method for operating a memory cell that is capable of storing multiple levels of charge, comprising:

programming the memory cell from each of a right side and a left side, the right side capable of storing a right bit and the left side capable of storing a left bit, a quantity of charge used in the programming of the memory cell setting when interaction between the right bit and the left bit is to exist, wherein the interaction between the right bit and the left bit exists when a higher charge is stored in the memory cell relative to lower charges that do not cause interaction between the right bit and the left bit; and

reading a charge level of the memory cell from a single side of the memory cell.

Claim 2 (Original): The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 1, wherein reading the charge level from the single side limits reading from one side of the memory cell to enable identification of the charge level.

Claim 3 (Original): The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 1, wherein the reading enables identification of the charge level when a read voltage is applied to a diffusion terminal of the single side of the memory cell and a ground voltage is applied to a diffusion terminal of the opposite side of the single side.

Claim 4 (Original): The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 3, wherein the read voltage is maintained below 2 volts.

Claim 5 (Canceled).

Claim 6 (Currently Amended): The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 1 ~~5~~, wherein four, eight, and sixteen memory states of the memory cell can be achieved through the combination of the right bit, the left bit, the quantity of charge, and the charge position.

Claim 7 (Original): The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 1, wherein increased programmed charge in the left bit causes the interaction between the right bit and the left bit, such that the right bit is induced to increase in correlation with increases in the programmed charge in the left bit.

Claim 8 (Original): The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 1, wherein higher threshold voltages of the memory cell can be achieved when the interaction between the right bit and the left bit of the memory cell exists relative to lower threshold voltages of the memory cell when no interaction between the right bit and the left bit of the memory cell exists.

Claim 9 (Currently Amended): The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 1, wherein the memory cell is a ~~NROM cell~~ charge trapping device.

Claim 10 (Currently Amended): A method for operating a memory cell that is capable of storing multiple levels of charge, comprising:

programming the memory cell from each of a first side and a second side, the first side capable of storing a first bit and the second side capable of storing a second bit, a quantity of charge used in the programming of the memory cell setting when interaction between the first bit and the second bit exists, wherein the interaction between the right bit and the left bit exists when a higher charge is stored in the memory cell relative to lower charge that do not cause interaction between the right bit and the left bit; and

reading a charge level of the memory cell from a single side of the memory cell.

Claim 11 (Original): The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 10, wherein the first side is a right side and the first bit is a right bit, and the second side is a left side and a second bit is a left bit.

Claim 12 (Original): The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 11, wherein reading the charge level from the

single side limits reading from one side of the memory cell to enable identification of the charge level.

Claim 13 (Original): The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 11, wherein the reading enables identification of the charge level when a read voltage is applied to a diffusion terminal of the single side of the memory cell and a ground voltage is applied to a diffusion terminal of the opposite side of the single side.

Claim 14 (Original): The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 13, wherein the read voltage is maintained below 2 volts.

Claim 15 (Canceled).

Claim 16 (Currently Amended): The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 10 ~~15~~, wherein four, eight, and sixteen memory states of the memory cell can be achieved through the combination of the right bit, the left bit, the quantity of charge, and the charge position.

Claim 17 (Original): The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 11, wherein increased programmed charge in the right bit causes the interaction between the right bit and the left bit, such that the left bit is induced to increase in correlation with increases in the programmed charge in the right bit.

Claim 18 (Original): The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 11, wherein higher threshold voltages of the memory cell can be achieved when the interaction between the right bit and the left bit of the memory cell exists relative to lower threshold voltages of the memory cell when no interaction between the right bit and the left bit of the memory cell exists.

Claim 19 (Currently Amended): The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 11, wherein the memory cell is a ~~NROM cell~~ charge trapping device.

Claim 20 (Original): The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 10, wherein the first side is a left side and the first bit is a left bit, and the second side is a right side and a second bit is a right bit.

Claim 21 (Original): The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 20, wherein reading the charge level from the single side limits reading from one side of the memory cell to enable identification of the charge level.

Claim 22 (Original): The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 20, wherein the reading enables identification of the charge level when a read voltage is applied to a diffusion terminal of the single side of the memory cell and a ground voltage is applied to a diffusion terminal of the opposite side of the single side.

Claim 23 (Original): The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 22, wherein the read voltage is maintained below 2 volts.

Claim 24 (Original): The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 20, wherein the interaction between the right bit and the left bit exists when a higher charge is stored in the memory cell relative to lower charge that do not cause interaction between the right bit and the left bit.

Claim 25 (Original): The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 24, wherein four, eight, and sixteen memory states of the memory cell can be achieved through the combination of the right bit, the left bit, the quantity of charge, and the charge position.

Claim 26 (Original): The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 20, wherein increased programmed charge in the right bit causes the interaction between the right bit and the left bit, such that the left bit is induced to increase in correlation with increases in the programmed charge in the right bit.

Claim 27 (Original): The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 20, wherein higher threshold voltages of the memory cell can be achieved when the interaction between the right bit and the left bit of the memory cell exists relative to lower threshold voltages of the memory cell when no interaction between the right bit and the left bit of the memory cell exists.

Claim 28 (Currently Amended): The method for operating a memory cell that is capable of storing multiple levels of charge as recited in claim 20, wherein the memory cell is a ~~NROM cell~~ charge trapping device.

Claim 29 (Canceled).